REMARKS

The Examiner's Action mailed on June 23, 2005 has been received and its contents carefully considered.

Claims 1-20 are pending in this application. Claims 1, 6, 9, 12, 15 and 18 are amended herein. Claims 1 and 12 remain the independent claims.

In the Action, claims 1-7 and 12-16 are rejected under 35 USC 102(a) as being anticipated by the Applicant's submitted prior art (figures 1-2, background of the invention, pages 1-4). Claims 8, 10-11, 17 and 19-20 are rejected under 35 USC 103(a) as being obvious over the Applicant's submitted prior art (figures 1-2, background of the invention, pages 1-4). Claims 8-11 and 17-20 are rejected under 35 USC 103(a) as being obvious over the Applicant's submitted prior art (figures 1-2, background of the invention, pages 1-4) in view of Habib et al. (U.S. Patent No. 6,903,583). Claims 1 and 12 are amended herein to more clearly distinguish over the applied prior art.

Claim 1, as amended, recites a method for verifying optimization of processor link for a system comprising a Northbridge, a bus coupled between a CPU and the Northbridge, and a Southbridge, the method comprising the steps of setting an initial bus width and an initial bus frequency of the bus coupled between the CPU and the Northbridge, wherein the bus operates at the initial bus width and the initial bus frequency; generating a read request to read the Southbridge; outputting of a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge when the Southbridge receives the read request; initializing a timer for calculating an elapsed time value and outputting an optimization verification signal with a first voltage level; outputting of a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value and transforming the voltage level of the optimization verification signal to a second voltage level; and reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal, wherein the bus operates thereafter at another bus operating bus width and another bus operating frequency.

Claim 12, as amended, recites a method for verifying optimization of processor link for a system comprising a Northbridge, a bus coupled between the CPU and the Northbridge, and a Southbridge, the method comprising the steps of setting an initial bus

width, an initial bus frequency, a bus operating bus width and a bus operating frequency of the bus coupled between the CPU and the Northbridge, wherein the bus operates at the initial bus width and the initial bus frequency; setting an optimized bus operating bus width and an optimized bus operating frequency of the bus; generating a read request to read the Southbridge; outputting of a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge when the Southbridge receiving the read request, initializing a timer for calculating an elapsed time value and outputting an optimization verification signal with a first voltage level; outputting of a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value and transforming the voltage level of the optimization verification signal to a second voltage level; and reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal, wherein the bus operates thereafter at the optimized bus operating bus width and the optimized bus operating frequency.

With respect to independent claim 1, the Examiner points to the Applicants' submitted prior art as disclosing all of the limitations of the claim. In particular, the Examiner asserts that Applicants submitted prior art discloses the steps of: outputting of a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge when the Southbridge receives the read request (page 3, lines 19-23); initializing a timer for calculating an elapsed time value and outputting an optimization verification signal with a first voltage level (page 3, lines 16-17); and outputting of a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value and transforming the voltage level of the optimization verification signal to a second voltage level (page 2, lines 22-29).

The Applicants respectfully disagree. What is discussed in the various sections of the specification referenced by the Examiner is the process in the prior art system whereby the LDT bus is disconnected when both the CPU and the Northbridge receive the asserted signal LDTSTOP#; the timer in the Southbridge begins to calculate an elapsed time value; and the Southbridge de-asserts the signal LDTSTOP# when the elapsed time value of the timer reaches a predetermined value. The de-asserting of the signal LDTSTOP# transforms the voltage level of the signal LDTSTOP# from the low level to the high-level. The LDT bus is reconnected when both the CPU and the Northbridge receive the de-

asserted signal LDTSTOP#. Thus, the Applicants' submitted prior art discloses only the recited bus disconnection signal (i.e., the asserted, low-level signal LDTSTOP#) and the recited bus connection signal (i.e., the de-asserted, high-level signal LDTSTOP#), but fails to teach or suggest the outputting of a distinct and separate optimization verification signal.

Further, Applicants' submitted prior art does not teach or suggest "transforming the voltage level of the optimization verification signal to a second voltage level", as claim 1 recites. Applicants' submitted prior art discloses only generation of a bus connection signal (LDTSTOP# with high voltage level) by transforming the voltage level of the bus disconnection signal, but not transformation of the voltage level of an optimization verification signal. Applicants' submitted prior art provides no mechanism for generating, let alone transforming, an optimization verification signal.

Claim 1 is amended herein to recite "reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal, wherein the bus operates thereafter at the optimized bus operating bus width and the optimized bus operating frequency" (emphasis added). This feature of the inventive method is disclosed, for example, in Figure 5, steps 30-32, and on page 9, lines 3-10 of the application. On the other hand, the Applicants, submitted prior art discloses that reconnection of the CPU and the Northbridge by the bus occurs in response only to the de-assertion of the signal LDTSTOP#, a signal which, as discussed above, is different from the optimization verification signal.

For the reasons discussed above, the Applicants respectfully submit that claim 1 patentably distinguishes over the prior art cited by the Examiner. Further, it is submitted that claims 2-11 are allowable for at least the reason that they depend from claim 1.

Independent claim 12 is rejected by the Examiner on essentially the same grounds as claim 1. The Applicants believe it should be clear from the above discussion that claim 12 also patentably distinguishes over the applied prior art. The Applicants also believe that claims 13-20 are allowable for at least the reason that they depend from claim 12.

Under MPEP2143, to establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. With respect to claims 8-11 and 17-20, the Examiner relies on the secondary reference, Habib, as teaching a signal level detecting circuit comprising a flip-flop and an OR logic

gate, the flip-flop outputs the optimization verification signal with the first voltage level when the Southbridge outputs the bus disconnection signal, and outputs the optimization verification signal with the second voltage level when the Southbridge outputs the bus connection signal; wherein the signal level detection circuit is coupled to the output terminal of the Southbridge; wherein the signal level detection circuit is coupled to the input terminals of the CPU or the Northbridge (figure 2; column 3, line 56 to column 4, line 58, and column 6, lines 14-32). The Examiner argues it would have been obvious to one of ordinary skill in the art to modify applicant's submitted prior art to include voltage level detecting circuit comprising a flip-flop and an OR logic gate, in order to control the voltage signal to optimize the bus width and operating frequency of the LTD bus.

The Applicants respectfully disagree. The figure and text in Habib referenced by the Examiner disclose a shutdown control circuit for a power supply that includes, among other things, inverters 210 and 212 and a D flip flop 214. However, there is no mention of an OR logic gate. As a result the shutdown control circuit in Habib is significantly different in structure and function from the signal level detection circuit of the present invention. It is submitted there would be no motivation for one of ordinary skill in the art to make the combination suggested by the Examiner. Accordingly, it is submitted that claims 8-11 and 17-20 recite limitations that patentably distinguish over the applied art combination, independent of independent claims 1 and 12.

Dependent claims 6, 9, 15 and 18-20 are amended herein to correct minor informalities, including missing punctuation and incorrect claim references.

In summary, it is submitted that this application, with claims 1-20, as amended, is in condition for allowance. Notice of allowance and the passing of this application to issue, are earnestly solicited.

[Concluded on next page]

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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Date

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